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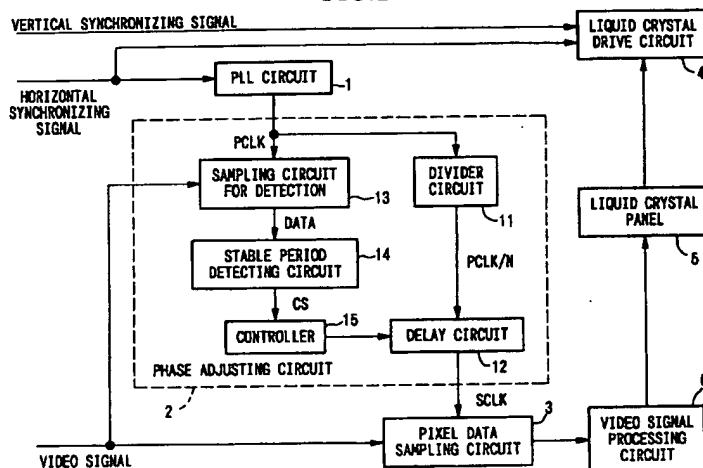
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(54) Data input circuit for a liquid crystal display device

(57) A liquid crystal display device is realized which facilitates the automatic display adjustment of moving images, and which effectively detects noise or the like interfering with the video signal. The liquid crystal display device is provided with: PLO circuit 1, which generates a standard clock (PCLK) which is synchronized with a horizontal synchronizing signal; a phase adjusting circuit 2, which includes a divider circuit 11, a delay circuit 12, a sampling circuit for detection 13, a stable period detecting circuit 14 and a controller 15, and which automatically phase of the standard clock (PCLK), and outputs a N divided sampling clock

(SCLK); a pixel data sampling circuit 3, into which the video signal is inputted, and which outputs sampling data obtained in accordance with the sampling clock (SCLK); a liquid crystal drive circuit 4, which outputs a liquid crystal drive signal; a video signal processing circuit 6, which conducts video processing including gamma correction, polarity inversion, and the like with respect to the sampling data; and a liquid crystal panel 5 into which the video processed image data are inputted, and which displays these data.

FIG.1



Description

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a liquid crystal display device, and in particular, relates to a liquid crystal display device into which video signals outputted from a personal computer or the like are inputted, and which displays the signals.

Description of Related Art

Conventionally, in this type of liquid crystal display device, the video signals which are to be displayed and which are outputted by a personal computer or the like differ from video signals in televisions or the like, in that these video signals are not completely continuously outputted, but are signals in which a fixed potential is maintained for each pixel; furthermore, in the corresponding liquid crystal display device itself, it is not the case that the video signal of one scanning line is continuously displayed, but rather a function is provided in which a video signal sampled pixel by pixel is displayed. This sampling function is provided in the liquid crystal display device; the video signal inputted from a personal computer or the like is displayed after being subjected to sampling within the liquid crystal display device. In the case in which the point at which the video signal is sampled within the liquid crystal display device is not the timing at which a fixed potential of the pixels is maintained, but rather the timing at which the pixels are switched, the following problems occur.

That is to say, there is a problem in that, because sampling of the inputted video signal is conducted at the point at which the potential changes, a constant sampling potential is not obtainable in the set up period or the hold period required in the sampling circuit, and the sampling potential becomes unstable. Furthermore, a situation is created in which, as a result of the influence of jitter in the sampling clock, pre-change pixel data may be sampled in a certain frame, while in the subsequent frame, post-change pixel data may be sampled. As a result of these phenomena, the edges of images in the liquid crystal display seem to flicker and the display quality of the images declines markedly. Accordingly, in such liquid crystal display devices, in order to ameliorate the decline in image quality by means of optimizing the sampling point, a circuit which regulates the phase of the sampling clock becomes necessary.

Figure 5 is a block diagram showing the structure of the essential parts of a conventional liquid crystal display device in which the adjustment of the sampling clock phase referred to above is performed by the user of the liquid crystal display device while observing the display screen. As shown in Figure 5, this conventional example is provided with: PLL circuit 1, which creates

and outputs a clock PCLK which is phase synchronized with a horizontal synchronizing signal; a phase adjusting circuit 2, which includes a phase adjusting switch 51 and a delay circuit 52, and which adjusts the phase of clock PCLK and outputs a clock SCLK; a sampling pixel data sampling circuit 3, into which a video signal is inputted, and which outputs sampling data via sampling clock SCLK; a liquid crystal drive circuit 4, into which a vertical synchronizing signal and the horizontal synchronizing signal are inputted, and which generates and outputs a liquid crystal display control signal; a liquid crystal panel 5, which displays the video signals which have been video processed; and a video signal processing circuit 6, which processes the sampling data. Normally, a dot clock is not outputted from a personal computer or the like; only a synchronizing signal is outputted. Accordingly, in this type of liquid crystal display device, in order to conduct the sampling of the video signal, a PLL circuit 1 which generates a clock PCLK which is synchronized with a the horizontal synchronizing signal is necessary, and this is provided as one of the essential structural elements above.

In Figure 5, PLL circuit 1 receives the input of the horizontal synchronizing signal, and a clock PCLK which is phase synchronized with the horizontal synchronizing signal is generated and inputted into delay circuit 52. In delay circuit 52, as a result of the manipulation of an operator conducted while viewing the display screen, the delay adjusted signal outputted from phase adjusting switch 51 is received, the phase delay amount of the clock PCLK is controlled and adjusted, and the phase adjusted sampling clock SCLK is outputted and this is inputted into pixel data sampling circuit 3. In pixel data sampling circuit 3, sampling clock SCLK is inputted, and via this sampling clock SCLK, the video signals R/G/B inputted from the personal computer are subjected to sampling. The sampling data output of pixel data sampling circuit 3 is inputted into video processing circuit 6, processing including gamma correction, polarity reversal, and the like is conducted, liquid crystal drive data are generated, these are inputted into liquid crystal panel 5, and display is conducted via the liquid crystal display control signal outputted from liquid crystal drive circuit 4. The liquid crystal display control signal receives the input of the vertical synchronizing signal and the horizontal synchronizing signal and is generated in liquid crystal drive circuit 4, and is inputted into liquid crystal panel 6.

Next, Figure 6 shows a block diagram of the structure of a different conventional phase adjusting circuit, disclosed in Japanese Patent Application, First Publication, No. Hei 7-219485. As shown in Figure 6, this phase adjusting circuit comprises: an adjustment initiation switch 66; a controller 63 which accepts as inputs a horizontal synchronizing signal, an operation initiation signal outputted from adjustment initiation switch 66, and a clock PCLK, and outputs a delay adjusting signal; a delay circuit 61, which accepts as inputs the delay

adjusting signal and the clock PCLK, and generates and outputs a sampling clock SCLK; an A/D converter 62, which accepts as inputs the sampling clock SCLK, a video signal, and the delay adjusting signal, and subjects the video signal to A/D conversion and outputs this; a memory 65, which accepts as inputs the A/D converted output of the A/D converter 62 and the delay adjusting signal, and which stores the A/D converted output; and a comparator circuit 64, which compares the A/D converted output of the A/D converter 62 and the output of memory 65, and transmits the results of this comparison to controller 63.

In Figure 6, the video signal inputted from a personal computer or the like is synchronized with sampling clock SCLK and subjected to sampling in A/D converter 62, and is also converted to a digital signal. The prespecified pixel data of a certain frame subjected to sampling in A/D converter 62 are temporarily stored in memory 65. The pixel data stored in memory 65 are compared in comparator circuit 64 with the pixel data corresponding to the same pixel in the subsequent frame, and any difference between these data is detected. In the case in which there was a difference in the results of the comparison, the phase of the sampling clock SCLK is determined to be inappropriate, and via the control function of controller 63, the delay amount in delay circuit 61 is controlled and adjusted, and a comparison of the sampling data is again conducted over a number of frames, and this is repeated until the results of the comparison are in agreement and no difference is generated. In the case of such agreement, the phase of the sampling clock SCLK is determined to be appropriate, and via the control function of controller 63, the delay amount of delay circuit 61 is fixed. The phase adjustment in this conventional example is only initiated when the adjustment initiation switch 66 is placed in the ON position by the operator; the controller 63 receives as an input the operation initiation signal outputted from adjustment initiation switch 66, and the control function of controller 63 commences, and after this, all operations are conducted automatically.

Figure 7 is a block diagram showing the structure of another conventional phase adjusting circuit, which was disclosed in Japanese Patent Application, First Publication, No. Hei 5-199483. As shown in Figure 7, this phase adjusting circuit is provided with an edge detecting circuit 71, which detects and outputs the beginning edge of the video signal, and a synchronizing signal 72, which accepts as inputs a clock PCLK and the edge detection output of the edge detecting circuit 71, and which generates and outputs a sampling clock SCLK.

In Figure 7, in edge detecting circuit 71, the edge of the video signal inputted from a personal computer or the like is detected, and a set pulse is outputted at a timing delayed by a prespecified period from the timing of this edge, and this set pulse is inputted into synchronizing circuit 72. In synchronizing circuit 72, the set pulse is accepted as input, the frequency of the clock PCLK syn-

chronized with the set pulse is N-divided, and a sampling clock SCLK is generated and outputted. By means of this, a sampling clock is obtained which is synchronized with the edge of the inputted video signal. In this case, as the division value N becomes larger in synchronizing circuit 72, it is possible to restrict the phase error to a smaller value, and N is commonly set to a value of 8 or more. Furthermore, by means of delaying the timing of the set pulse by a prespecified amount from the edge, the phase difference between the video signal and the sampling clock SCLK is fixed and optimized, and thereby the adjustment of the sampling point may be realized automatically.

In the conventional liquid crystal display devices described above, in the case of the conventional example shown in Figure 5, the operator manipulates a switch while viewing the display screen, and thereby, the timing adjustment of the sampling clock SCLK is conducted, but there is a disadvantage in that the manipulations of the operator may become complex.

Furthermore, in the conventional phase adjusting circuit shown in Figure 6, by means of conducting a comparison of the sampling data of the video data corresponding to a certain pixel frame by frame, the timing adjustment of the sampling point with respect to the video signal is conducted; however, in the case of moving images in which the display screen changes frame by frame, the inputted video signal changes with each frame, and a comparison between frame units will never result in agreement, and it is thus impossible to conduct optimal timing adjustment, and this represents a drawback in that the displayed images during adjustment are limited to still images.

In this conventional example, it is not possible to continuously conduct adjustment, so that a switch operation is also necessary in order to initiate adjustment, and this has the additional drawback that this operation is complex, and furthermore, in the timing adjustment, a number of frame intervals are required, so that time is required for the timing adjustment.

Furthermore, in the conventional phase adjusting circuit shown in Figure 7, the edge of the video signal is detected, and synchronization is conducted with respect to a set pulse which is delayed by a prespecified time from the edge detection signal, and thereby, the timing of the sampling point is adjusted; however, in cases in which, as a result of the personal computer or the like outputting the video signal which is to be displayed, the wave-form of differing video signals becomes disordered as a result of noise or the like originating in ringing or reflection or the like, and this affects the timing of the set pulse delayed by a predetermined period from the edge, it becomes impossible to guarantee the set up time required in the sampling circuit of the pixel data, and the timing of the sampling point is not set to the appropriate timing. Additionally, when the level of the noise or the like arising from ringing or reflection or the like of the video signal is high, edge detection is con-

ducted with respect to the wave form of this noise or the like in the edge detecting circuit, and it becomes impossible to optimally adjust the sampling point.

SUMMARY OF THE INVENTION

The first liquid crystal display device of the present invention comprises a liquid crystal display device which is provided with: a phase synchronizing circuit, into which a horizontal synchronizing signal is inputted and which generates and outputs a standard clock signal synchronized with the horizontal synchronizing signal; a phase adjusting circuit into which a specified video signal which is to be displayed is inputted, and which, via the standard clock signal outputted from the phase synchronizing circuit, generates and outputs a sampling clock signal having an appropriate phase for sampling pixel data of the video signal; a pixel data sampling circuit, into which the video signal is inputted and which samples the pixel data of the video signal via the sampling clock signal, and generates and outputs sampling image data; a video processing circuit, which conducts video processing with respect to the sampling image data, and generates and output image data for image display; and a liquid crystal panel into which image data for image display is inputted, and which displays these data; wherein the phase adjusting circuit is provided with: a sampling circuit for detection, into which the video signal is inputted, and which conducts the sampling of the video signal via the standard clock signal, and which outputs first sampling data for potential level determination period detection; a stable period detecting circuit, into which the first sampling data is inputted, and which detects the presence or absence of potential changes in each sampling point adjoining the sampling data, and which generates and outputs a signal indicating the potential stable period of the first sampling data from the results of the detection; a divider circuit, into which the standard clock signal is inputted, and which divides the frequency of the standard clock signal and generates and outputs a divided clock signal; a controller, which accepts as input the signal showing the potential stable period of the first sampling data, and which counts the periods in which the potential change of the video signal is stable, with reference to the signal indicating the potential stable periods, and on the basis of the results of this count, makes a determination as to whether the set up period and hold period, which are set in advance as necessary conditions for the image data sampling function, can be guaranteed, and in the case of a determination that it is possible to guarantee the necessary conditions, calculates the phase after the set up period from the stable initiation point of the potential level, and with reference to the results of this calculation, generates and outputs a control signal for phase control with respect to the divided clock signal; and a delay circuit, into which the divided clock signal outputted from the divider circuit is inputted, and which con-

trols and adjusts the phase of the divided clock signal via the control signal outputted from the controller, and outputs this to the image data sampling circuit as a second sampling clock signal.

Furthermore, the second liquid crystal display device of the present invention comprises a liquid crystal display device which is provided with: a phase synchronizing circuit into which a horizontal synchronizing signal is inputted and which generates and outputs a standard clock signal synchronized with the horizontal synchronizing signal; a phase adjusting circuit, into which a specified video signal which is to be displayed is inputted, and which, via the standard clock signal outputted from the phase synchronizing circuit, generates and outputs a sampling clock signal having an appropriate phase for sampling pixel data of the video signal; a pixel data sampling circuit, into which the video signal is inputted and which samples the pixel data of the video signal via the sampling clock signal, and generates and outputs sampling image data; a video processing circuit, which conducts video processing with respect to the sampling image data, and generates and output image data for image display; and a liquid crystal panel into which image data for image display is inputted, and which displays these data; wherein the phase adjusting circuit is provided with: a sampling clock generating circuit for detection, into which the standard clock signal is inputted, which breaks down the standard clock signal into a number m ($m:0, 1, 2, \dots, m$) of standard clock signals, and with respect to the various standard clock signals, with the phase amount when the cycle of the standard clock signal is divided into m represented by \cdot , generates and outputs a number m of sampling clock signals which are formed so as to provide the various delay phase amounts of m .; a sampling circuit for detection, into which the video signal is inputted, and which samples, via the number m of sampling clock signals, the periods corresponding to one pixel of the video data at number m of sampling points, and generates and outputs a number m of corresponding sampling data; a stable period detecting circuit, into which the number m of sampling data are inputted, and which detects the presence or absence of a change in potential at each sampling point adjoining the number m of sampling data, and based on the results of this detection, generates and outputs a signal indicating the potential stable period of each sampling data; a controller, which accepts as an input the signal indicating the potential stable period of each sampling data, counts the periods at which the potential change of the video data is stable with reference to the signal showing the potential stable periods, and using the results of this count, makes a determination as to whether it is possible to guarantee the set up period and hold period which are set in advance as necessary conditions of the image data sampling function, and in the case in which a determination is made that it is possible to guarantee the necessary conditions, calculates the phase after the set up

period from the stable initiation point of the potential level, and with reference to the results of this calculation, outputs a control signal for phase control with respect to the sampling clock signal of the image data; and a selecting circuit, into which are inputted the number m of sampling clock signals outputted from the sampling clock generating circuit for detection, and which, by means of the control signal, selects and outputs the sampling clock signal having the optimal phase relationship from among the number m of sampling clock signals.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram showing the structure of a first embodiment of the present invention.

Figure 2 is an operational timing diagram relating to the first embodiment.

Figure 3 is a block diagram showing the structure of a second embodiment of the present invention.

Figure 4 is an operational timing diagram relating to the second embodiment.

Figure 5 is a block diagram showing the structure of a conventional example.

Figure 6 is a block diagram showing the structure of a phase adjusting circuit in accordance with another conventional example.

Figure 7 is a block diagram showing the structure of a phase adjusting circuit in accordance with another conventional example.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Next, the present invention will be explained with reference to the diagrams.

Figure 1 is a block diagram showing the structure of the essential parts of a first embodiment of the present invention. As is shown in Figure 1, the present embodiment is provided with: a PLL circuit 1, which generates and outputs a standard clock (PCLK) synchronized with the horizontal synchronizing signal; a phase adjusting circuit 2, including a divider circuit 11, a delay circuit 12, a sampling circuit for detection 13, a stable period detecting circuit 14, and a controller 15, which accepts as inputs the video signal and the standard clock (PCLK), adjusts the phase of the standard clock (PCLK), and generates and outputs a sampling clock (SCLK), the frequency of which is divided to $1/N$ (where N is a positive integer); a pixel data sampling circuit 3, into which the video signal is inputted, and which outputs sampling data via the sampling clock (SCLK); a liquid crystal drive circuit 4, into which the vertical synchronizing signal and the horizontal synchronizing signal are inputted, and which generates and outputs a liquid crystal drive signal; a video signal processing circuit 6, which conducts video processing including gamma correction and polarity reversal and the like with

respect to the sampling data outputted from pixel data sampling circuit 3; and a liquid crystal panel 5, into which are inputted the image data processed in the video signal processing circuit 6, and which displays these data via the liquid crystal drive signal.

Furthermore, Figures 2(a), (b), (c), (d), and (e) are timing diagrams showing each signal in the present embodiment: Figure 2(a) indicates the standard clock (PCLK) outputted from the PLL circuit 1, Figure 2(b) shows the inputted video signal (continuous waveform display) and the sampling data (DATA: dot display) outputted from sampling circuit 13 for detection, Figure 2(c) indicates the signal (CS) indicating the stable period outputted by stable period detecting circuit 14, Figure 2(d) indicates the divided clock (PCLK/16) outputted by the divider circuit 11 when the dividing value N is 16, and Figure 2(e) indicates the sampling clock (SCLK) outputted by the delay circuit 12.

Hereinbelow, with references to Figures 1 and 2, the operation of the present embodiment will be explained in the case in which the dividing value N of the divider circuit 11 is 16. Accordingly, the divided clock (PCLK/ N) outputted from the divider circuit 11 shown in Figure 1 is replaced with a divided clock (PCLK/16) for the explanation of the operation.

In Figure 1, PLL circuit 1 accepts the horizontal synchronizing signal as an input, and a standard clock (PCLK: see Figure 2(a)) is generated which is phase synchronized with the horizontal synchronizing circuit, and this is inputted into the divider circuit 11 and the sampling circuit for detection 13 within the phase adjusting circuit 2. In divider circuit 11, the frequency of the sampling clock (PCLK) is divided by 16, and a divided clock (PCLK/16: see Figure 2(b)) is generated, and this is inputted into delay circuit 12. Furthermore, in sampling circuit for detection 13, the inputted video signal (see the continuous wave form of Figure 2(b)) is sampled via the standard clock (PCLK), and the sampling data of the video signal (DATA: see the dot display of Figure 2(b)) is outputted and inputted into stable period detecting circuit 14. In stable period detecting circuit 14, the sampling data (DATA) outputted by sampling circuit for detection 13 are accepted as inputs, and a comparison of the level values of the sampling potentials at two adjoining sampling points is repeatedly conducted. In this way, by repeatedly conducting a comparison of adjoining sampling potentials, the presence or absence of potential changes in the inputted sampling data (DATA) is detected, and using the results of this detection, a signal (CS: see Figure 2(c)) showing the potential stable periods of the sampling data (DATA) is outputted, and this is inputted into controller 15. In controller 15, the signal (CS) is accepted as input, and with reference to this signal (CS), a count is conducted of the periods in which there is no change in potential in the inputted video signal, so that it is stable, and from the results of this count, in pixel data sampling circuit 3, when a determination has been made that it is possible to guarantee

the necessary set up period and hold period which are set in advance, then the phase after the set up period which is set in advance is calculated from the initiation point of the stable period of the potential level, and a control signal corresponding to the results of this calculation is outputted and inputted into delay circuit 12. In delay circuit 12, the divided clock (PCLK/16) outputted from the divider circuit 11 is accepted as input, and the delay amount of the divided clock (PCLK/16) is adjusted to the appropriate amount by means of the control signal inputted by controller 15, and a sampling clock in which the frequency is divided by 16 (SCLK: see Figure 2(e)) is generated, and this is inputted into pixel data sampling circuit 3. In pixel data sampling circuit 3, the video signal inputted from the personal computer or the like is sampled via this sampling clock (SCLK), and the sampling data output is inputted into video processing circuit 6. In video processing circuit 6, as described above, processing which includes gamma correction and polarity inversion and the like is conducted with respect to the sampling data, and image data for liquid crystal display are generated and outputted, these data are inputted into liquid crystal panel 5, and these data are displayed via the liquid crystal drive signal outputted by liquid crystal drive circuit 4.

In the embodiment described above, the explanation centered on the case in which the dividing value N in divider circuit 11 had a value of 16; however, the dividing value N exerts an influence on the number of sampling points used for stable period detection, that is to say, on the smallest unit of stable period detection, and this value also determines the adjustment precision, so that when this value N is too small, there is no adjustment effect, and it is thus necessary that N be set to the maximum value which will permit circuit operation, and a value of at least 16 is desirable.

In addition, in the comparison determination of the sampling potential in stable period detecting circuit 14, the detection precision which is required depends on the number of display colors of the video signal which is inputted; precision which permits the detection of differences in potential in each of the unit gradations of R, G, and B is necessary. For example, if the video signal inputted is 0.7 Vpp, then in the case of the display of 256 color gradations, precision sufficient to discriminate differences of 2.7 mV is required.

Next, with respect to the operation of phase adjusting circuit 2 shown in Figure 1, this will be explained with reference to the timing diagrams shown in Figure 2(a), (b), (c), (d), and (e).

As described previously, the display of the continuous wave form shown in the timing diagram of Figure 2(b) indicates the video signal inputted from a personal computer or the like; however, the continuous pixel data of this video signal are displayed as wave forms formed as black, white, black. With respect to this video signal, in sampling circuit for detection 13, each potential of the video signal is sampled at sampling points from VS₀ to

VS₁₅, as shown in Figure 2(b), in accordance with the standard clock (PCLK) shown in Figure 2(a). The sampling data (DATA) at each of these sampling points are inputted into the stable period detecting circuit 14, and the various adjoining potentials of the sampling points VS₀ and VS₁, VS₁ and VS₂, VS₂ and VS₃, VS₃ and VS₄, ..., VS₁₄ and VS₁₅ are compared, and when as a result of this comparison the potentials are at the same level, a binary signal indicating an "H" level is generated, and as shown in Figure 2(c), this is outputted as signal (CS) and inputted into controller 15. In controller 15, the time T_A during which the signal (CS) is maintained at an "H" level is counted, and this is compared with the set up time and the hold time which are required in the pixel data sampling circuit 3 and are pre-set, and the quality of the inputted video signal is evaluated in controller 15. Furthermore, with respect to the phase after the passage of the set up time T_B, which is required in the pixel data sampling circuit 3 and is pre-set, from the beginning of the signal (CS), the delay amount T_C required to bring the timing of the sampling clock (SCLK) for pixel sampling into conformity with this is calculated in controller 15. Then, by applying the delay amount T_C which was calculated with respect to the divided clock (PCLK/16) inputted from divider circuit 11, a sampling clock (SCLK) for pixel data sampling which provides an appropriate phase is generated and outputted in delay circuit 12, as shown in Figure 2(e).

Figure 3 is a block diagram showing the structure of the phase adjusting circuit in a second embodiment of the present invention. As is shown in Figure 3, the phase adjusting circuit 2 of the present embodiment is provided with: a sampling clock generating circuit for detection 21, into which a standard clock (PCLK) which is synchronized with a horizontal synchronizing signal is inputted, and which divides this standard clock (PCLK) into a number m (a positive integer) of standard clocks, and which applies, with respect to these standard clocks, a delay amount proportional to the amount of the cycle thereof divided by m, and which generates and outputs, in stages, a number m of sampling clocks for detection (DPCLK[0,1,2,...,m]) having different phases; a sampling circuit for detection 23, which accepts as an input the sampling clocks for detection (DPCLK[0, 1, 2, ..., M]), and which is formed from a number m of sampling circuits which sample, at a number m of points, intervals corresponding to each pixel of the video signal inputted from a personal computer or the like via the sampling clocks for detection (DPCLK[0, 1, 2, ..., m]); a stable period detecting circuit 24, which includes a number m of comparator circuits which conduct a comparison of sampling potentials at a number m of adjoining pairs of sampling points of the sampling data outputted from a number m of sampling circuits, and which detects the presence or absence of a change in potential of the video signals which are inputted, and in the case in which there is no change in the potential and the signal is stable, outputs a signal (CS[0, 1, 2, ..., M])

indicating the potential stable period of the corresponding sampling data; a controller 25, which accepts as inputs the signals (CS[0, 1, 2, ..., M]), and with reference to these signals (CS[0, 1, 2, ..., M]), conducts a count of the intervals in which there is no change in potential in the inputted video signal and the signal is stable, and by means of the results of this count, when a determination has been made, in the pixel data sampling circuit (not shown in Figure 3; see the pixel data sampling circuit 3 of Figure 1), that it is possible to guarantee the necessary set up time and hold time which were preset, the phase after the preset setup time from the point of initiation of the stable period of the potential level is calculated, and the controller generates and outputs a control signal which serves to select, from among the number m of sampling clocks for detection corresponding to the results of the calculations, the sampling clock which has the optimal phase relationship; and a selecting circuit 22, which accepts as an input the sampling clocks for detection (DPCLK[0, 1, 2, ..., m]) which were outputted by the sampling clock generating circuit for detection 21, controls these by means of the control signal, selects the appropriate sampling clock for detection from among these, and outputs this as the sampling clock (SCLK) to the pixel data sampling circuit. The value of m described above has an effect on the number of sampling points used for stable period detection, or in other words, has an effect on the smallest unit of stable period detection, and this value determines the precision of phase adjustment. Accordingly, when the value of m is too small, the adjustment effect is lost, so that it is desirable that this value be set to the maximum value at which the circuit can operate, and a value of at least 16 is desirable.

Next, using 16 as the value of m, the operation of the phase adjusting circuit shown in Figure 3 will be explained with reference to the timing diagrams shown in Figures 4(a), (b), (c), (d), (e), (f), (g), (h), (i), (j), (k), (l), and (p).

The continuous wave form display shown in the timing diagram of Figure 4(g) indicates the video signal which is inputted from a personal computer or the like; the continuous pixel data are displayed as a wave form which is formed in a black, white, black manner. A number m of sampling clocks for detection (DPCLK[0, 1, 2, ..., m]) is outputted from sampling clock generating circuit for detection 21, as shown in Figures 4(b), (c), (d), (e), ..., and these are inputted into sampling circuit for detection 23. With respect to the inputted video signals, the potentials of the video signal at each sampling point from VS₀ to VS₁₅ are sampled in sampling circuit 23 for detection, as shown by the dot display in Figure 4(g), by means of the number m of sampling clocks for detection (DPCLK[0, 1, ..., m]), and the sampling data (DATA) at these sampling points are inputted into stable period detecting circuit 24. The potentials of adjoining sampling points VS₀ and VS₁, VS₁ and VS₂, VS₂ and VS₃, VS₃ and VS₄, ..., VS₁₄ and VS₁₅ are compared in

the 16 comparator circuits, and in the case in which as a result of these comparisons, the potential was at the same level, signal (CS[10]), signal (CS[11]), ..., and signal (CS[15]), are generated in stable period detecting circuit 24 as binary signals indicating an "H" level, as shown in Figures 4(j), (k), ..., (l), and these signals are outputted. In the case of the signal (CS[0]) and the signal (CS[1]) shown in Figures 4(h) and (k), the potential does not have the same level at the corresponding sampling points, so that a binary signal indicating an "L" level is generated. The "H" level signals (CS) are inputted into delay circuit 12, and from the number of these "H" level signals (CS), the periods are counted at which the inputted video signal was stable, and in a manner similar to that of the first embodiment, a comparison is conducted of the set up time and hold time necessary in the pixel data sampling circuit which was preset, and a determination is made with respect to the quality of the inputted video signal. Furthermore, as can be seen from Figures 4(j), (k), and (l), the initiation timing during which the signal was stable is detected from the "H" level signals (CS) outputted from the stable period detecting circuit 24, and the phase after the set up time required in the pixel data sampling circuit which was preset is calculated. Additionally, a control signal which operates so as to select the sampling clock for detection having the closest phase relationship to this calculated phase is outputted by controller 25, and by means of this control signal, in selecting circuit 22, the sampling clock for detection having the closest phase relationship is selected on the basis of the results of this calculation from among the sampling clocks for detection outputted by the sampling clock generating circuit for detection 21, and as shown in Figure 4(p), this is outputted as a sampling clock signal (SCLK).

As explained above, in the present invention, in a freely selected display screen including moving images, sampling is conducted with respect to the data of one pixel of the inputted video signal by means of a sampling clock having a frequency higher than the dot clock frequency of the video signal, the potential changes in the video signal are observed in detail, potential level fluctuations and subsequent stability of the signal wave form are detected, the appropriate phase with respect to the video signal is calculated, and the automatic phase adjustment of the sampling clock of the pixel data is conducted with reference to the results of this calculation, and thereby, it is possible to conduct normal liquid crystal display in a rapid manner without requiring operational control by a human being.

Furthermore, as described above, sampling is conducted by means of a sampling clock having a frequency higher than that of the dot clock of the video signal, and the potential changes of the video signal are observed in detail, and thereby, wave form variations in the inputted video signal resulting from differing interfering ringing, noise, or the like, and stable periods in which there are no fluctuations in the potential level, are

detected, and the appropriate phase is calculated via a comparison between the stable periods and the desired sampling period of the pixel data, and an automatic phase adjustment of the pixel data sampling clock is conducted with reference to the results of this calculation, and thereby, the quality of the wave form variations resulting from the ringing or noise described above can be ascertained, and the automatic phase adjustment of the sampling clock can be conducted without affecting the length of the unstable periods resulting from ringing or noise or the like, and thereby it is possible to conduct normal liquid crystal display.

Claims

1. A liquid crystal display device which is provided with: a phase synchronizing circuit, into which a horizontal synchronizing signal is inputted and which generates and outputs a standard clock signal synchronized with the horizontal synchronizing signal; a phase adjusting circuit into which a specified video signal which is to be displayed is inputted, and which, via the standard clock signal outputted from the phase synchronizing circuit, generates and outputs a sampling clock signal having an appropriate phase for sampling pixel data of the video signal; a pixel data sampling circuit, into which the video signal is inputted and which samples the pixel data of the video signal via the sampling clock signal, and generates and outputs sampling image data; a video processing circuit, which conducts video processing with respect to the sampling image data, and generates and output image data for image display; and a liquid crystal panel into which image data for image display is inputted, and which displays these data;

wherein the phase adjusting circuit is provided with:

- a sampling circuit for detection, into which the video signal is inputted, and which conducts the sampling of the video signal via the standard clock signal, and which outputs first sampling data for potential level determination period detection;
- a stable period detecting circuit, into which the first sampling data is inputted, and which detects the presence or absence of potential changes in each sampling point adjoining the sampling data, and which generates and outputs a signal indicating the potential stable period of the first sampling data from the results of the detection;
- a divider circuit, into which the standard clock signal is inputted, and which divides the frequency of the standard clock signal and generates and outputs a divided clock signal;
- a controller, which accepts as input the signal

showing the potential stable period of the first sampling data, and which counts the periods in which the potential change of the video signal is stable, with reference to the signal indicating the potential stable periods, and on the basis of the results of this count, makes a determination as to whether the set up period and hold period, which are set in advance as necessary conditions for the image data sampling function, can be guaranteed, and in the case of a determination that it is possible to guarantee the necessary conditions, calculates the phase after the set up period from the stable initiation point of the potential level, and with reference to the results of this calculation, generates and outputs a control signal for phase control with respect to the divided clock signal; and

a delay circuit, into which the divided clock signal outputted from the divider circuit is inputted, and which controls and adjusts the phase of the divided clock signal via the control signal outputted from the controller, and outputs this to the image data sampling circuit as a second sampling clock signal.

2. A liquid crystal display device which is provided with: a phase synchronizing circuit into which a horizontal synchronizing signal is inputted and which generates and outputs a standard clock signal synchronized with the horizontal synchronizing signal; a phase adjusting circuit, into which a specified video signal which is to be displayed is inputted, and which, via the standard clock signal outputted from the phase synchronizing circuit, generates and outputs a sampling clock signal having an appropriate phase for sampling pixel data of the video signal; a pixel data sampling circuit, into which the video signal is inputted and which samples the pixel data of the video signal via the sampling clock signal, and generates and outputs sampling image data; a video processing circuit, which conducts video processing with respect to the sampling image data, and generates and output image data for image display; and a liquid crystal panel into which image data for image display is inputted, and which displays these data;

wherein the phase adjusting circuit is provided with:

- a sampling clock generating circuit for detection, into which the standard clock signal is inputted, which breaks down the standard clock signal into a number m ($m: 0, 1, 2, \dots, m$) of standard clock signals, and with respect to the various standard clock signals, with the phase amount when the cycle of the standard clock signal is divided into m represented by \cdot , generates and outputs a number m of sampling

clock signals which are formed so as to provide the various delay phase amounts of m ;

a sampling circuit for detection, into which the video signal is inputted, and which samples, via the number m of sampling clock signals, the periods corresponding to one pixel of the video data at number m of sampling points, and generates and outputs a number m of corresponding sampling data;

a stable period detecting circuit, into which the number m of sampling data are inputted, and which detects the presence or absence of a change in potential at each sampling point adjoining the number m of sampling data, and based on the results of this detection, generates and outputs a signal indicating the potential stable period of each sampling data;

a controller, which accepts as an input the signal indicating the potential stable period of each sampling data, counts the periods at which the potential change of the video data is stable with reference to the signal showing the potential stable periods, and using the results of this count, makes a determination as to whether it is possible to guarantee the set up period and hold period which are set in advance as necessary conditions of the image data sampling function, and in the case in which a determination is made that it is possible to guarantee the necessary conditions, calculates the phase after the set up period from the stable initiation point of the potential level, and with reference to the results of this calculation, outputs a control signal for phase control with respect to the sampling clock signal of the image data; and

a selecting circuit, into which are inputted the number m of sampling clock signals outputted from the sampling clock generating circuit for detection, and which, by means of the control signal, selects and outputs the sampling clock signal having the optimal phase relationship from among the number m of sampling clock signals.

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FIG.1

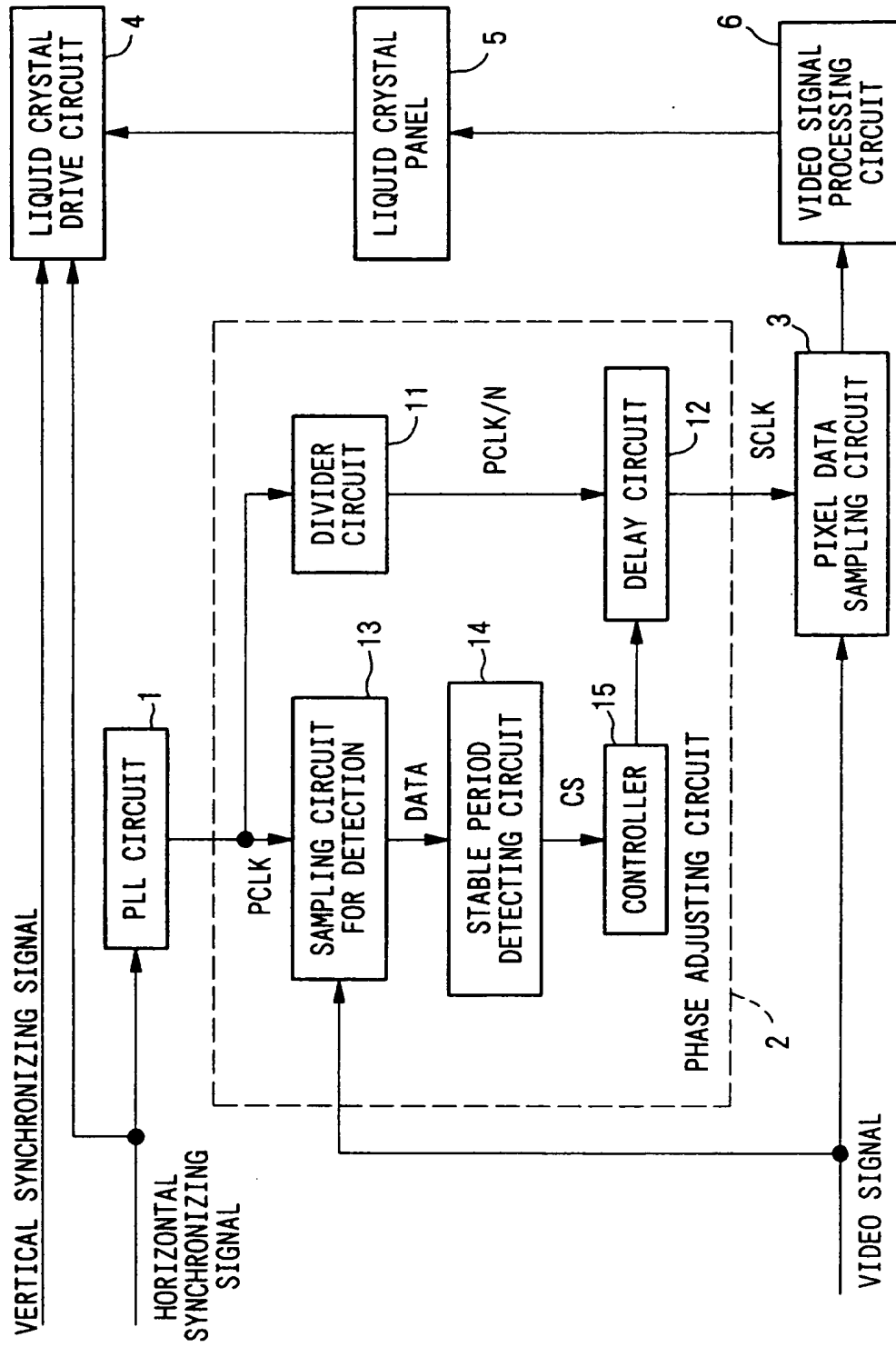


FIG.2

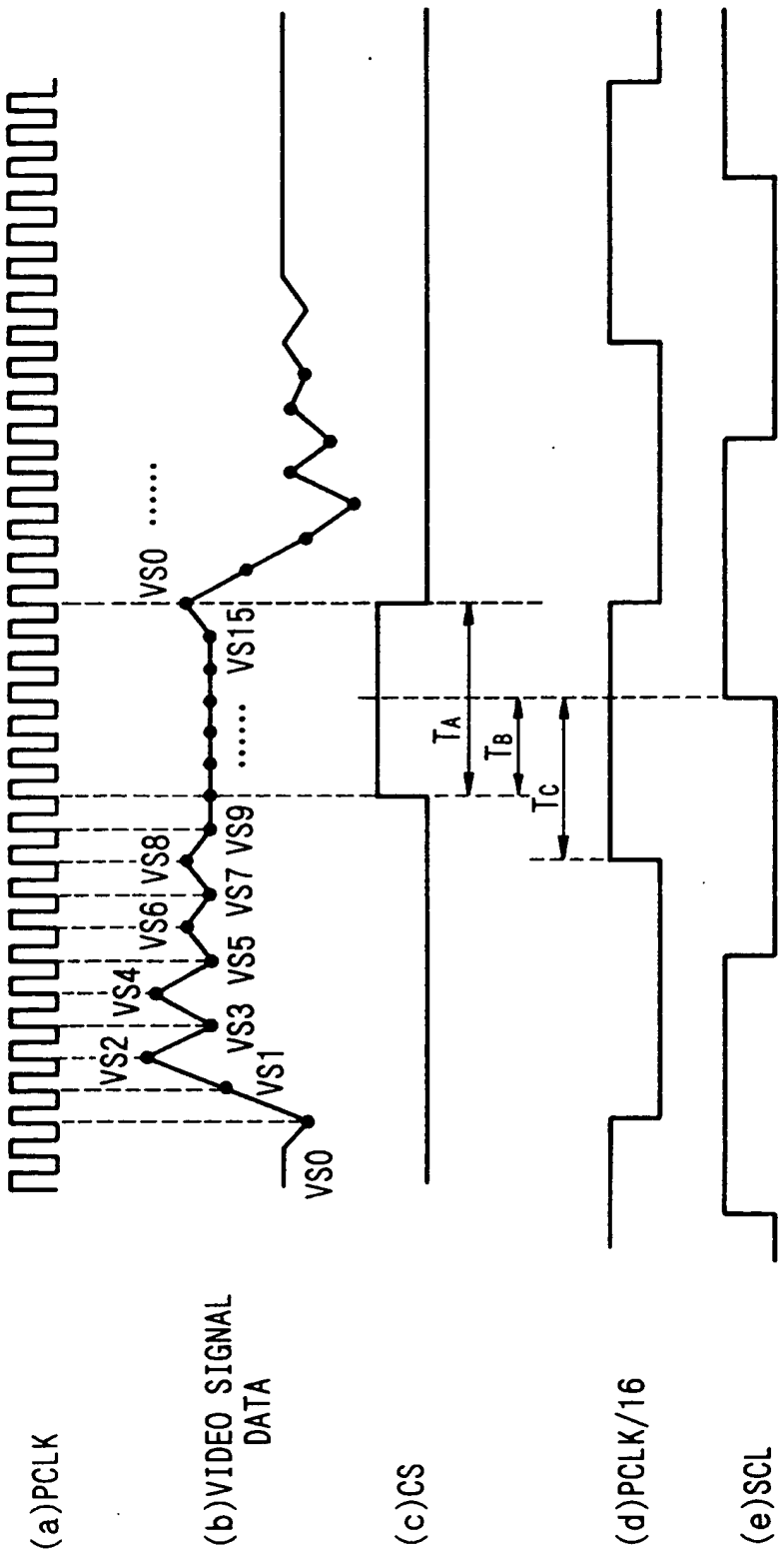


FIG.3

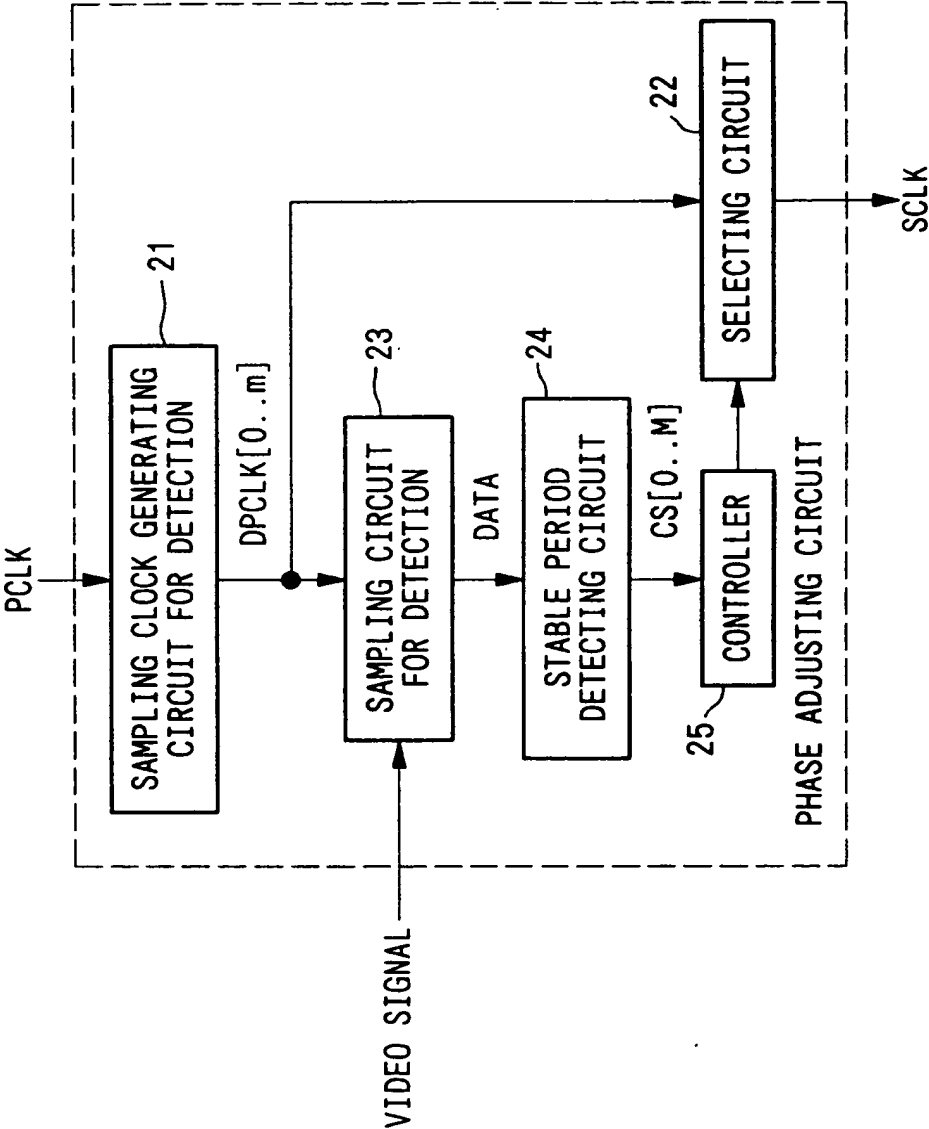


FIG.4

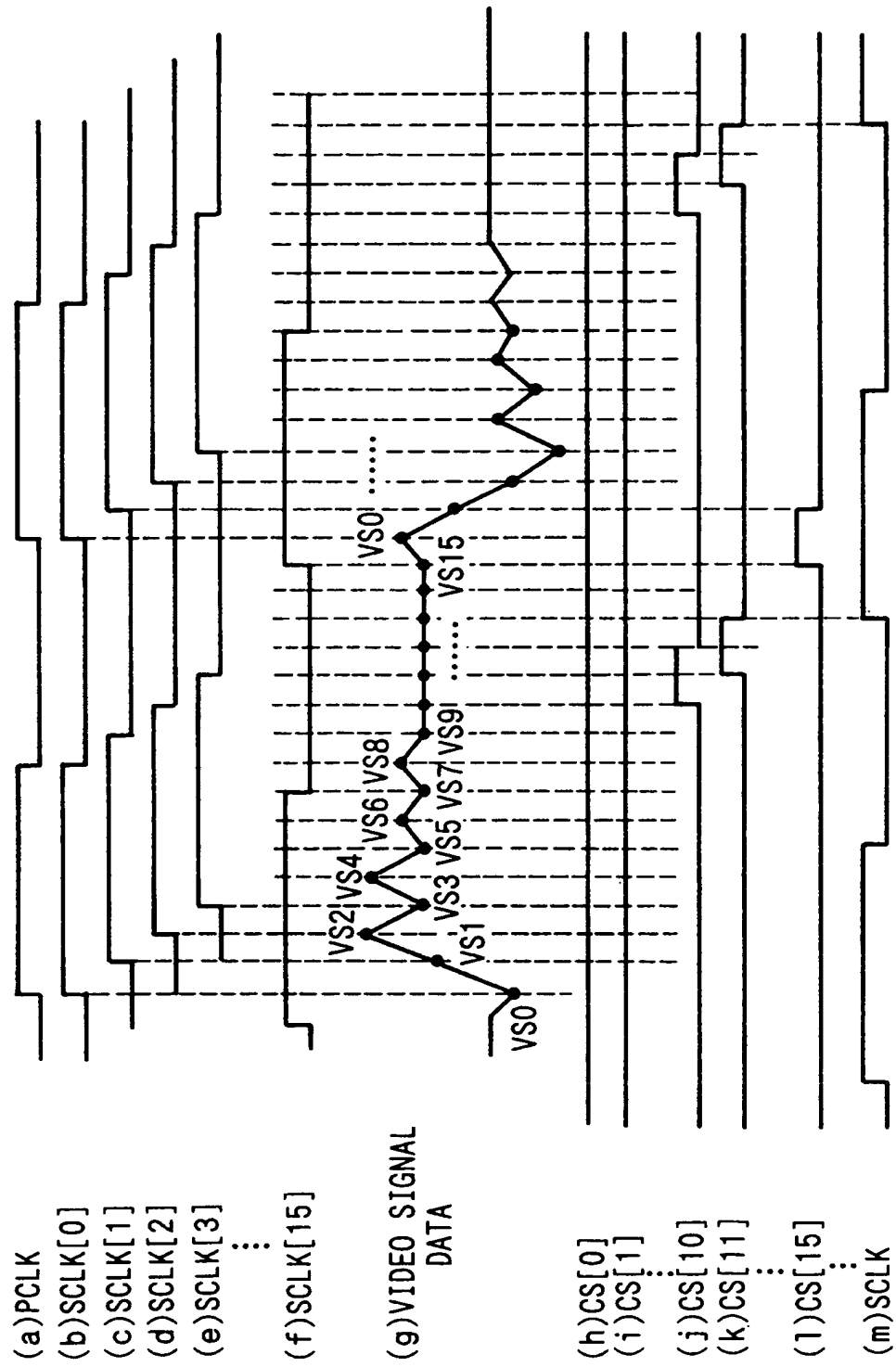


FIG.5

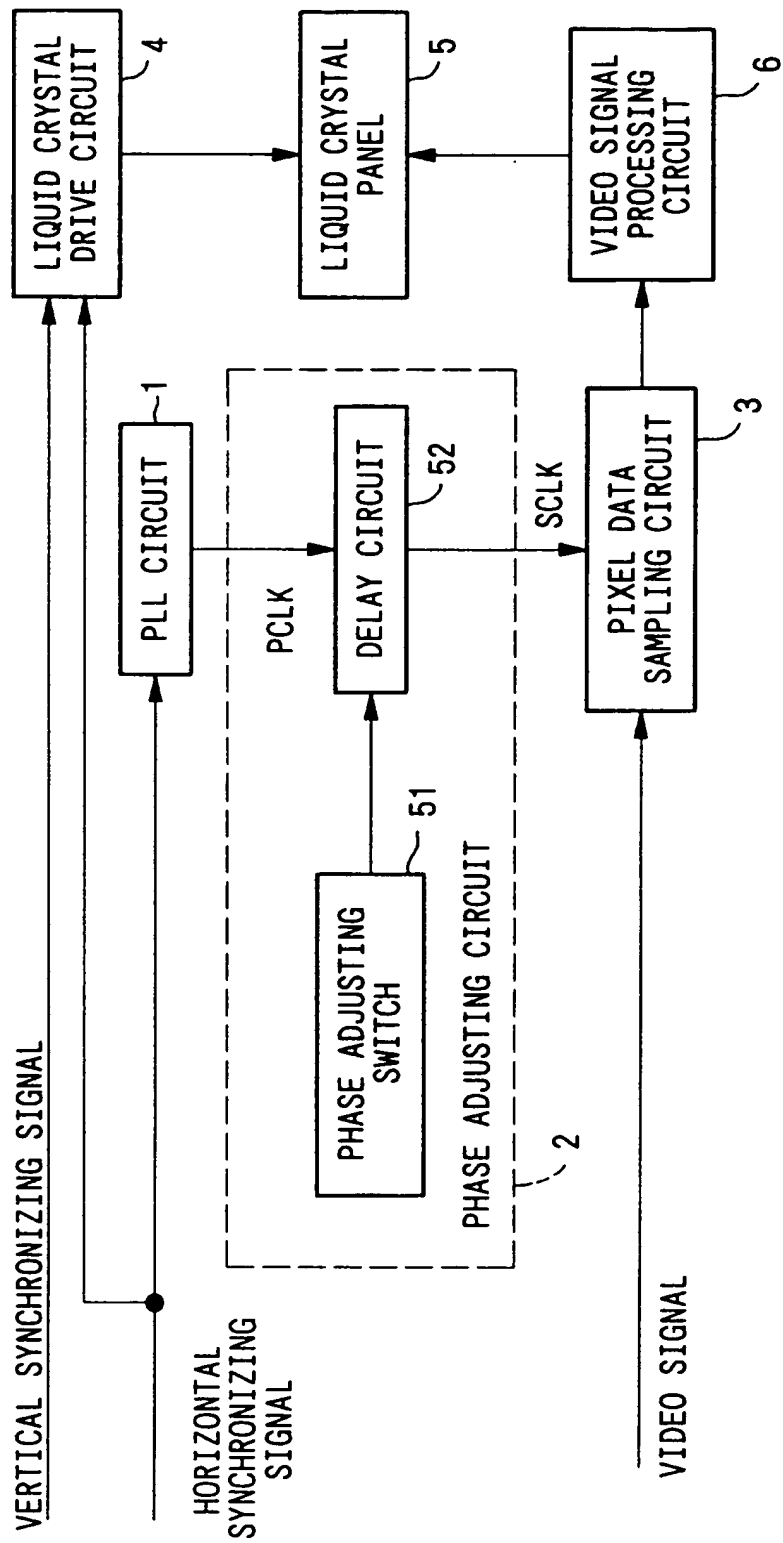


FIG. 6

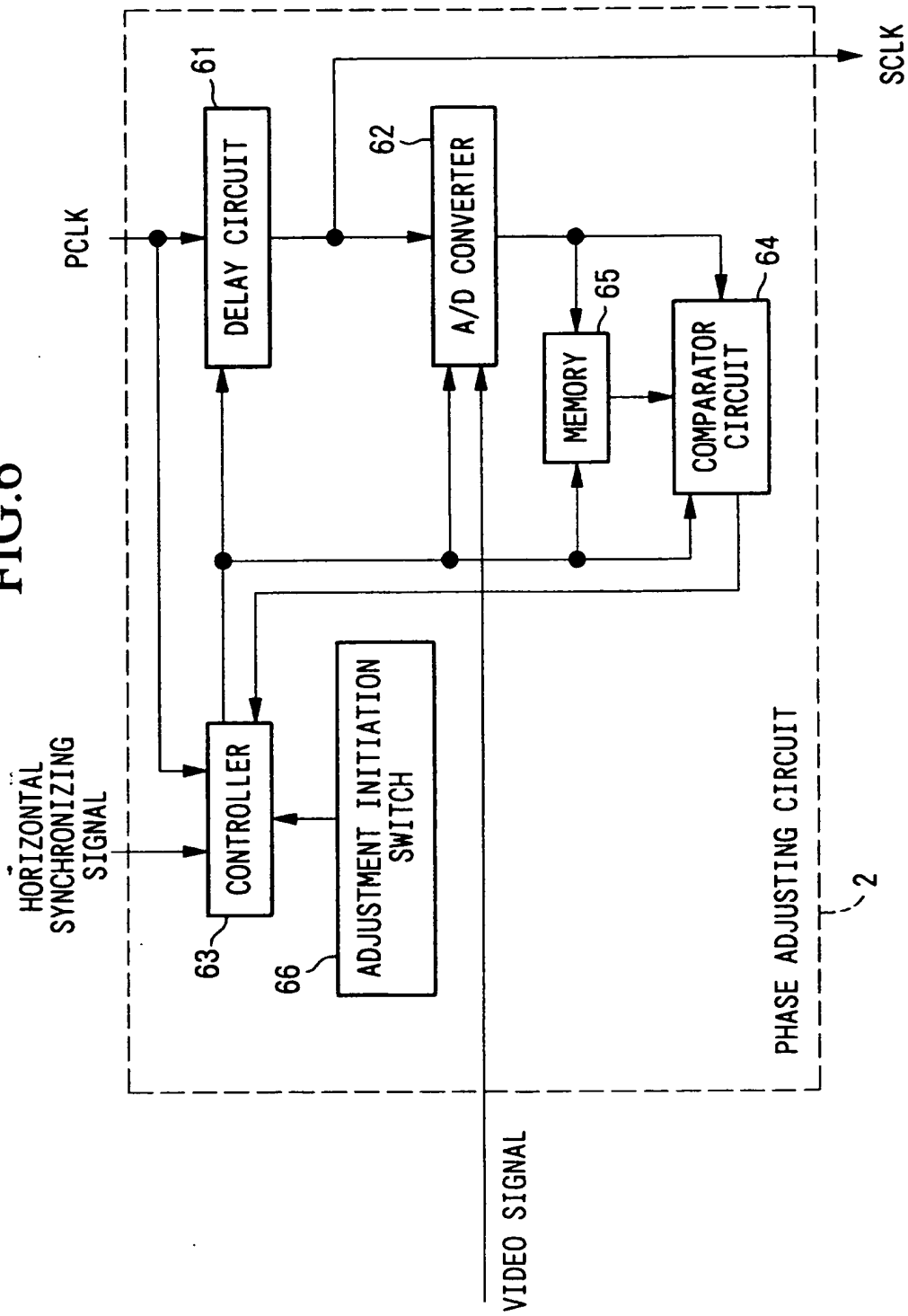
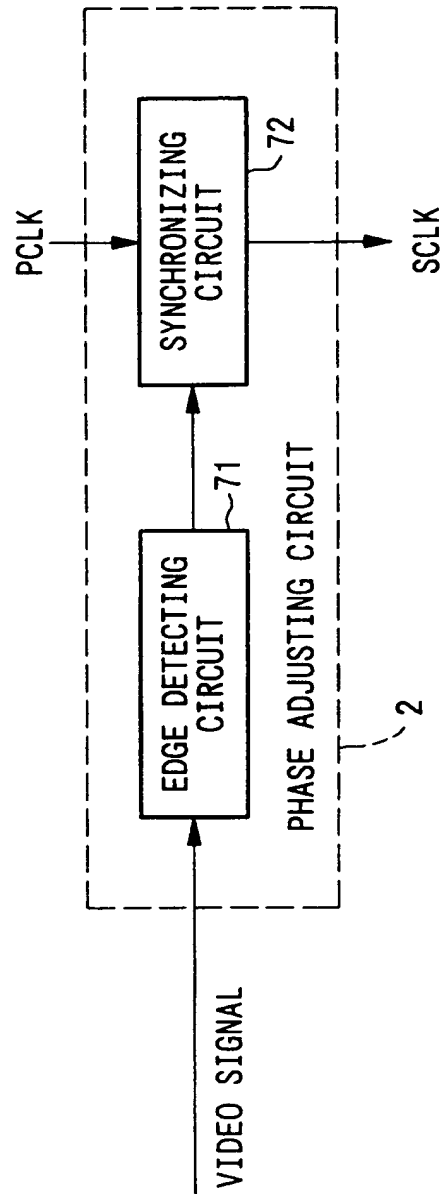


FIG. 7





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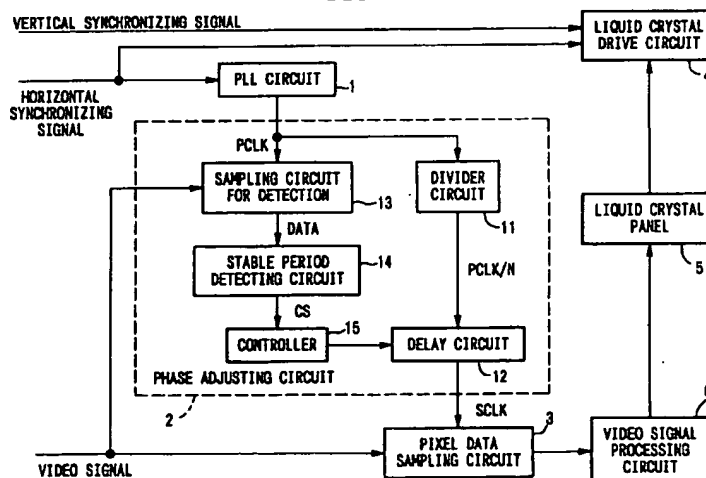
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Tokyo (JP)

(54) **Data input circuit for a liquid crystal display device**

(57) A liquid crystal display device is realized which facilitates the automatic display adjustment of moving images, and which effectively detects noise or the like interfering with the video signal. The liquid crystal display device is provided with : PLO circuit 1, which generates a standard clock (PCLK) which is synchronized with a horizontal synchronizing signal; a phase adjusting circuit 2, which includes a divider circuit 11, a delay circuit 12, a sampling circuit for detection 13, a stable period detecting circuit 14 and a controller 15, and which automatically phase of the standard clock (PCLK), and outputs a N divided sampling clock

(SCLK); a pixel data sampling circuit 3, into which the video signal is inputted, and which outputs sampling data obtained in accordance with the sampling clock (SCLK); a liquid crystal drive circuit 4, which outputs a liquid crystal drive signal; a video signal processing circuit 6, which conducts video processing including gamma correction, polarity inversion, and the like with respect to the sampling data; and a liquid crystal panel 5 into which the video processed image data are inputted, and which displays these data.

FIG.1





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DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	EP 0 577 841 A (FANUC LTD.) 12 January 1994	1	G09G3/36 G09G3/20
A	* Abstract * * column 1, line 12 - column 2, line 30; figures 1-4 * * column 4, line 12 - column 7, line 18 *	2	
A	--- "Automatic Phase Adjustment" IBM TECHNICAL DISCLOSURE BULLETIN., vol. 37, no. 5, May 1994, pages 203-204, XP000453131 NEW YORK US	1	
X	* Whole article *	2	
A	--- PATENT ABSTRACTS OF JAPAN vol. 17, no. 70 (P-1485), 12 February 1993 -& JP 04 276791 A (SHARP CO.), 1 October 1992 * abstract *	1,2	
A,P	--- EP 0 791 913 A (SEIKO EPSON CO.) 27 August 1997 * Abstract * * page 2, line 14 - page 3, line 15; figures 40-42C * * page 7, line 48 - page 10, line 38; figures 1-10 *	1,2	TECHNICAL FIELDS SEARCHED (Int.Cl.6) G09G
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 5 October 1998	Examiner Corsi, F
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	

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